



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re Application of

Tetsushi TANIZAKI

Serial No.: 10/649,682

Filed: August 28, 2003

For: SEMICONDUCTOR MEMORY DEVICE PERMITTING BOUNDARY SCAN TEST

: Customer Number: 20277

: Confirmation Number: 5653

: Group Art Unit: 2818

: Examiner:

REQUEST FOR CORRECTED FILING RECEIPT

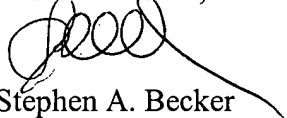
Mail Stop: Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is a copy of the Filing Receipt received from the U.S. Patent and Trademark Office in the above-referenced application. It is noted that the Attorney Docket Number is incorrect. The Attorney Docket Number should read 67161-079. It is requested that a corrected filing receipt be issued.

Respectfully submitted,

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67161 - 079

APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/649,682	08/28/2003	2818	750	—20277	10	5	1

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CONFIRMATION NO. 5653

FILING RECEIPT



OC000000011342056

Date Mailed: 11/24/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Tetsushi Tanizaki, Hyogo, JAPAN;

Assignment For Published Patent Application

RENESAS TECHNOLOGY CORP.;

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2003-069416(P) 03/14/2003

If Required, Foreign Filing License Granted: 11/22/2003

Projected Publication Date: 09/16/2004

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor memory device permitting boundary scan test

Preliminary Class

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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